CLAIMS

1. A source synchronous link comprising:

a communication link;

a source synchronous receiver coupled to said communication link; and

a source synchronous transmitter coupled to said communication link, including,

data transmit logic configured to manage the transmission of data signals over a data line of said communication link; and

data strobe transmit logic configured to generate a one or more data strobe signals over a clock line of said communication link, wherein said data strobe transmit logic halts each said one or more data strobe signals in a logical state in response to an external condition.

2. The source synchronous link of claim 1, wherein said one or more data strobe signals comprise a first data strobe signal and a second data strobe signal transmitted with a phase opposite a phase of said first frequency.

3. The source synchronous link of claim 1, wherein said first data strobe signal and said second data strobe signal may be transmitted at either one of two logical states and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said one or more data strobe signals.

4. A source synchronous transmitter constructed and arranged to transmit a differential data strobe over a source synchronous link at a first frequency, with the differential data strobe signals toggling between one of two logical states at said first frequency when operating in a normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation.

5. A debug system to determine whether source synchronous receiver has properly captured data transmitted from a transmitter, comprising:
a source synchronous transmitter;
a source synchronous receiver;
a debug system configured to control said transmitter to transmit data and a data strobe at a first frequency and to transmit a debug bit pattern while holding said differential data strobe at a predetermined logic level;
a data capture storage and analysis device configured to scan said receiver to retrieve and store captured data for comparison with said debug bit pattern.

6. The source synchronous link of claim 4, wherein said transmitter comprises:
a differential data strobe transmit logic configured to generate said differential data strobe comprising a data strobe signal and an inverse data strobe signal;
a differential data strobe signal generator configured to determine a said logical states of said data strobe and said inverse data strobe signals;
a strobe stopping logic that controls said logic level signals utilized by said signal generator to cause said data strobe and said inverse data strobe signals to remain halted in a desired logical state.

7. In a source synchronous communication system, a method for determining whether a source synchronous link receiver properly captured data transmitted by a source synchronous transmitter, the method comprising the steps of:
a) transmitting by the transmitter a data signal at a first clock frequency;
b) transmitting by the transmitter concurrently with said step a), at least one data strobe signal at a second clock frequency, wherein said data strobe signal alternates between a high logical state and a low logical state during each data strobe cycle;
c) receiving, by the transmitter, a command to halt the data strobe signal; and
d) maintaining, by the transmitter in response to said command, said one or more data strobe signals transmitted by said transmitter at one logical state.

8. The method of claim 7, further comprising the step of:

e) prior to said step d), receiving an indication of the logical state in which to maintain said data strobe signal, and

wherein said one logical state at which said one or more data strobe signals are held, is said logical state indicated in said step e).

9. In a source synchronous system, a method for determining whether a source synchronous receiver has properly captured data transmitted from a source synchronous transmitter, the method comprising the steps of:

selecting a bit pattern to transmit over communication link coupling said transmitter and said receiver;

causing the transmitter to halt differential data strobe and to transmit concurrently said predetermined bit pattern to the receiver;

scanning data capture flip-flops in the source synchronous receiver to retrieve captured bit pattern;

storing said captured data; and

comparing said captured data with said transmitted bit pattern.

10. The method of claim 9, wherein said step of selecting comprises the steps of:

writing said predetermined bit patterns to a memory; and

retrieving a selected predetermined bit pattern from the memory.

11. A differential data strobe transmitter for generating a differential data strobe comprising a data strobe signal and an inverse data strobe signal over a communication link with a data signal, comprising:

a differential data strobe signal generator that determines a shape of said data strobe signal and said inverse data strobe signal waveforms; and

strobe stopping logic configured to control signal level states used by said signal generator logic to cause said data strobe signal and said inverse data strobe signal to remain halted in a desired logical state.

12. The differential data strobe transmitter of claim 11, wherein said differential data strobe signal generator logic selects alternately between two applied signal levels to generate each said data strobe signal and said inverse data strobe signal.

13. The differential data strobe transmitter of claim 12, wherein said differential data strobe signal generator receives as inputs a first and a second logic level signal for selection to generate said data strobe signal and a third and fourth logic level signals for selection to generate said inverse data strobe signal.

14. The differential data strobe transmitter of claim 12,

wherein during normal operations, said differential data strobe is not halted, said first and third input signals are held consistently in an asserted state while said second of fourth input signals are held consistently in a de-asserted state,

wherein said signal generator selects alternately said first and said second input signals to generate said data strobe signal at a first clock frequency, and between said third and said fourth input signals to generate said inverse data strobe signal at said first clock frequency.

15. The differential data strobe transmitter of claim 12, wherein said data strobe signal and said inverse data strobe signal are each generated as single ended bits that are opposite in phase with each other.

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